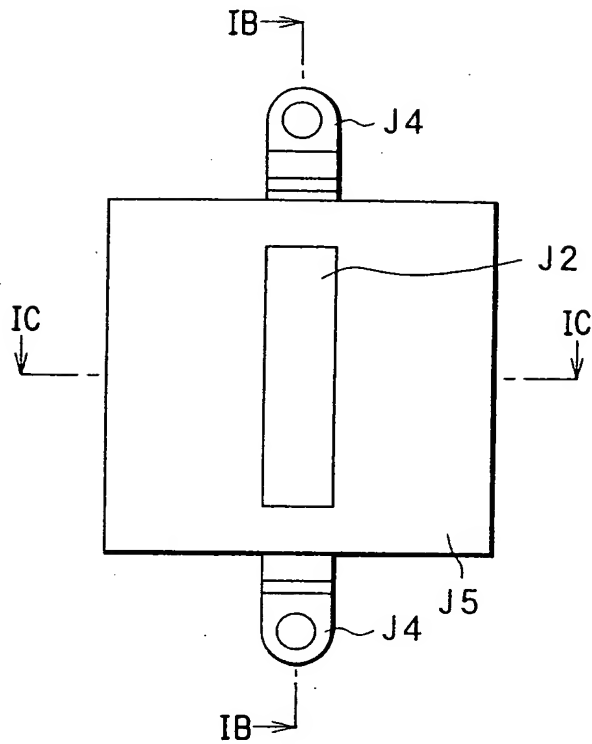


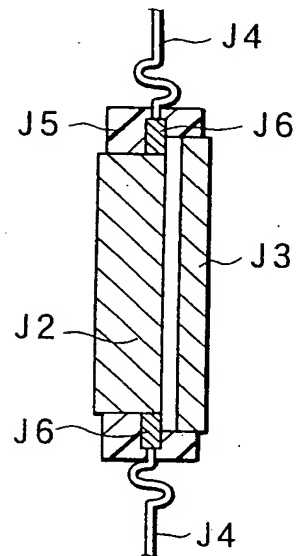
**FIG. 1A**

PRIOR ART



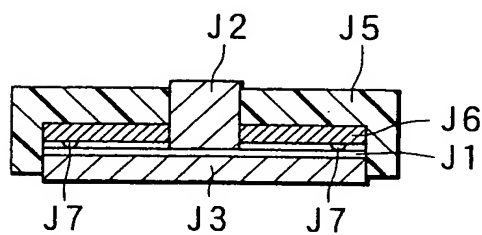
**FIG. 1B**

PRIOR ART



**FIG. 1C**

PRIOR ART



A cross-sectional view of a semiconductor device. The device consists of a central channel region (1a) flanked by two doped regions (4). Above the channel is a layer (2a) and a top layer (2). Below the channel is another doped region (4) and a bottom layer (3). A central region (6a) is defined by a vertical line, and a bottom region (6b) is defined by a horizontal line. A force vector (F) is applied to the top layer (2). A dashed line (9) and a curved arrow (B) indicate a bending or deformation of the structure. A region (7) is shown on the right side, with a curved arrow indicating a movement or deformation.

# FIG. 3

NAME OF METAL	CHEMICAL COMPOSITION (%)													
	Fe	Zn	P	Ni	Si	Sn	NiB	Mn	Mg	Cr	Ti	B	Cu	Al
METAL a	2.3	0.1	0.03										REMAIN.	
METAL b	2.4	0.12	0.03										REMAIN.	
METAL c				3.0	0.7								REMAIN.	
METAL d	1.5	0.5				0.5							REMAIN.	
METAL e	1.0	0.05	0.1			1.0							REMAIN.	
METAL f	0.75		0.03			1.25							REMAIN.	
METAL g	0.05 0.15		0.025 0.040										REMAIN.	
METAL h	0.05 0.4		0.05 0.1			0.05 0.2	0.05 0.45						REMAIN.	
METAL i			0.15 OR LOWER	0.1 0.4		1.7 2.3							REMAIN.	
METAL j		0.2 0.35		3.0 3.4	0.6 0.75	1.0 1.5							REMAIN.	
METAL k	0.12 1.0	0.03 0.1			0.1 1.0			0.02 0.05	0.02 0.05		0.02 0.05		0.03 0.2	REMAIN.
METAL l	0.5	0.1			0.3 0.7			0.05	0.35 0.5	0.03		0.06	0.1	REMAIN.

FIG. 4A

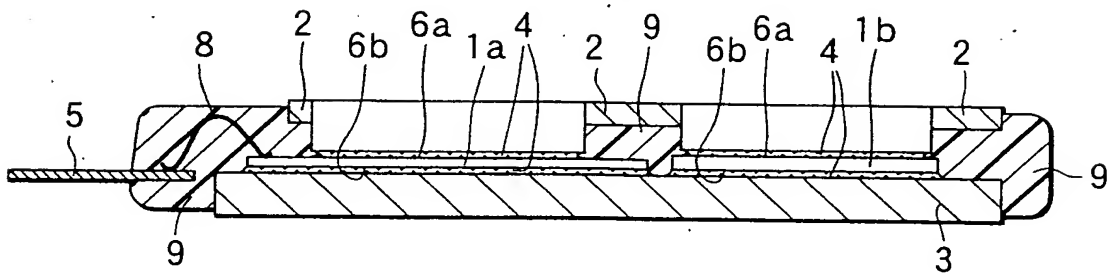


FIG. 4B

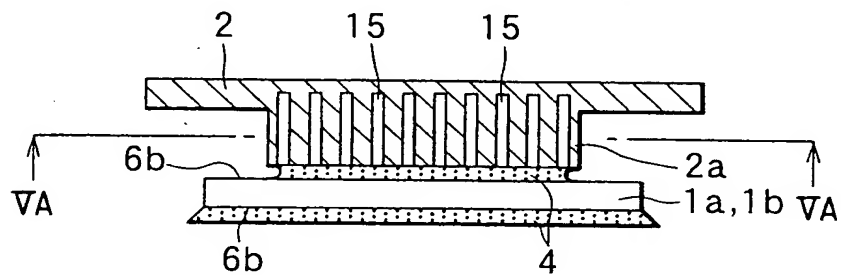


FIG. 4C

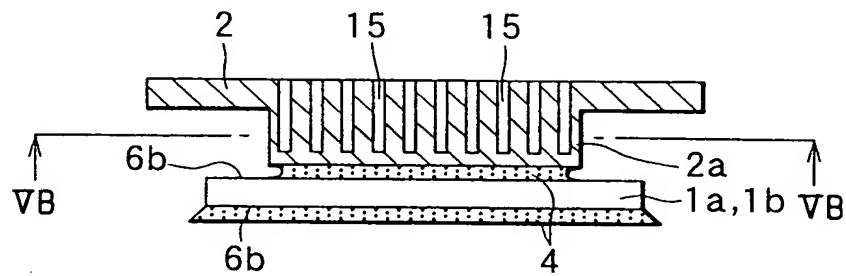
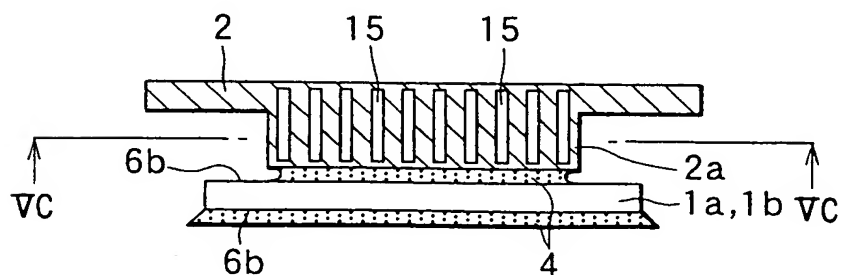
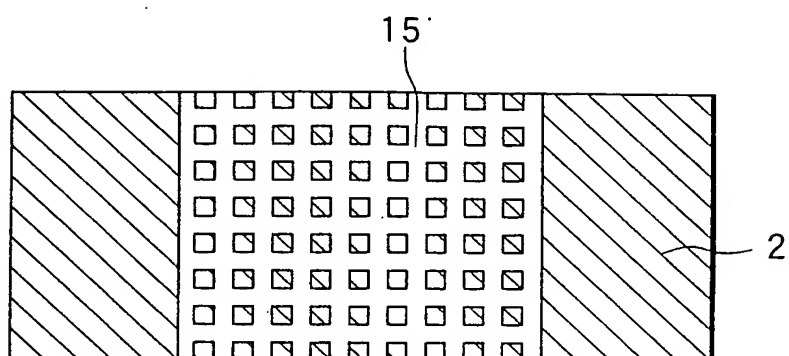


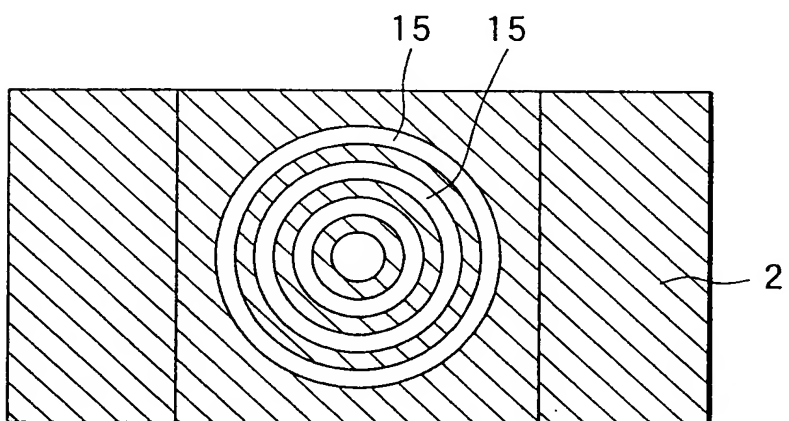
FIG. 4D



**FIG. 5A**



**FIG. 5B**



**FIG. 5C**

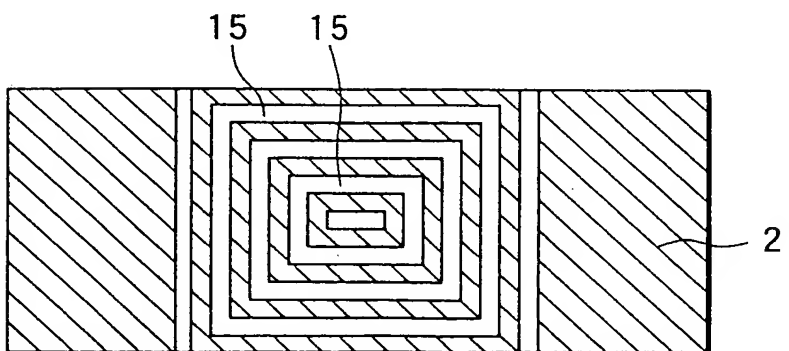


FIG. 6

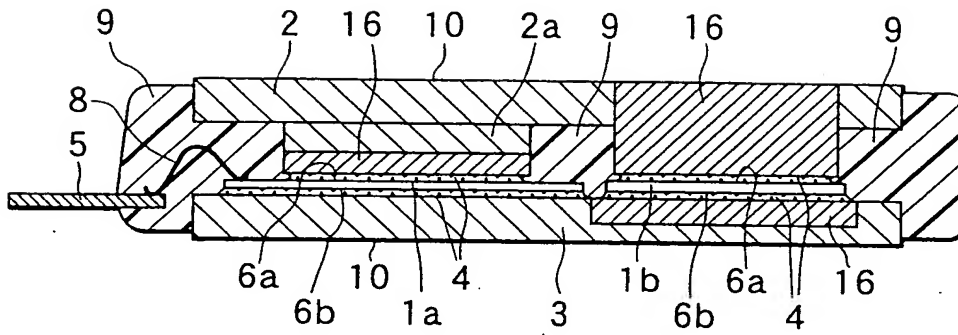


FIG. 7

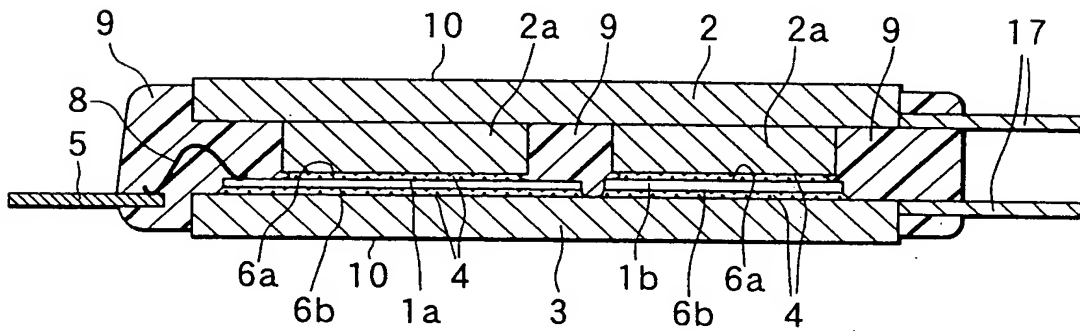
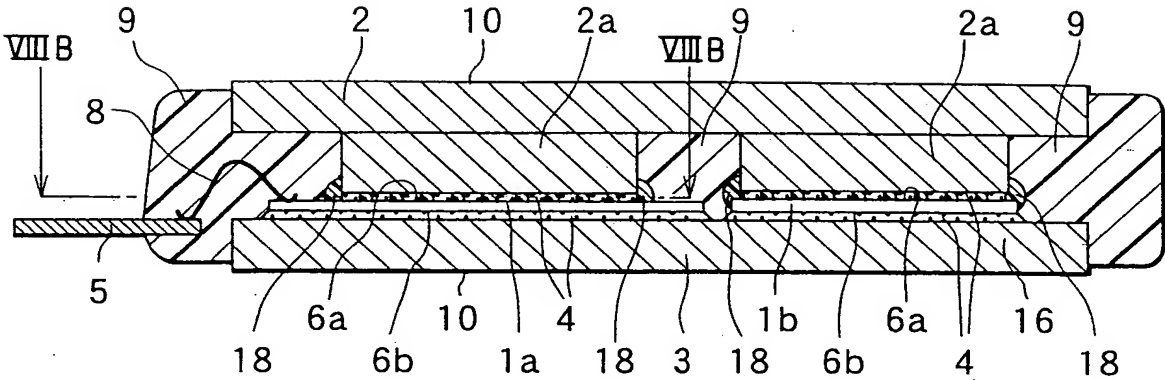


FIG. 8A



**FIG. 8B**

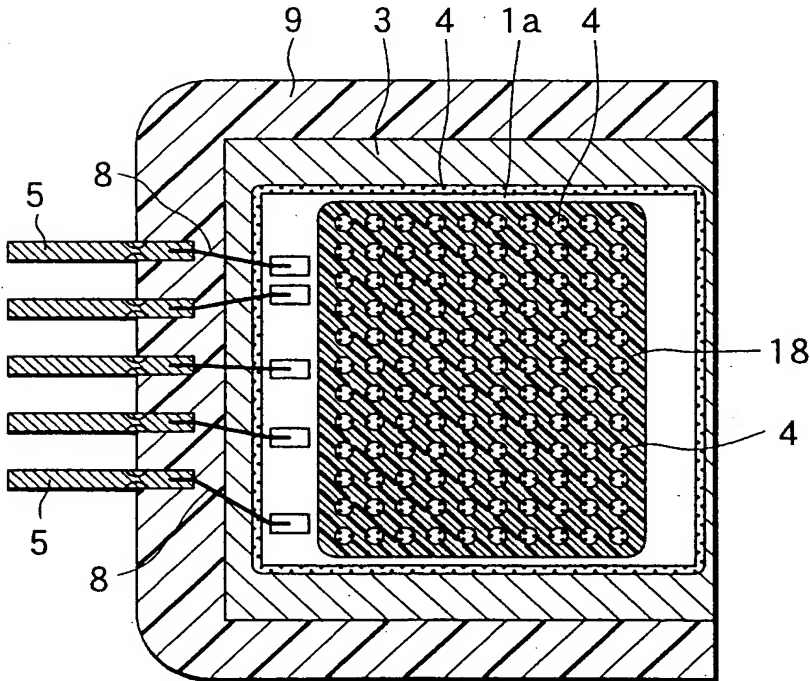


FIG. 9A

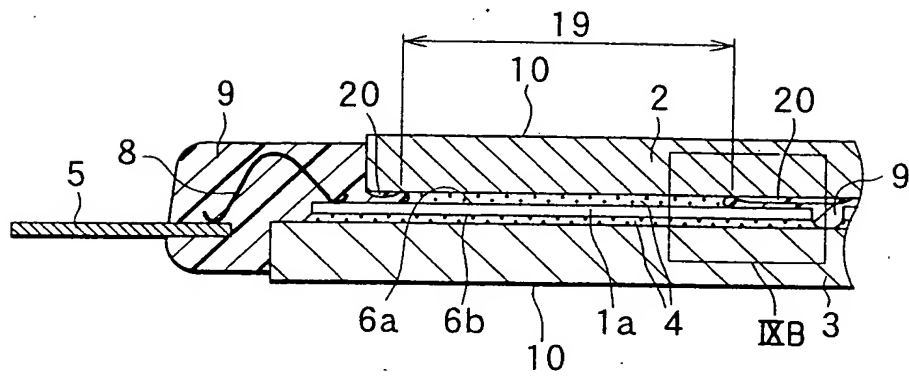


FIG. 9B

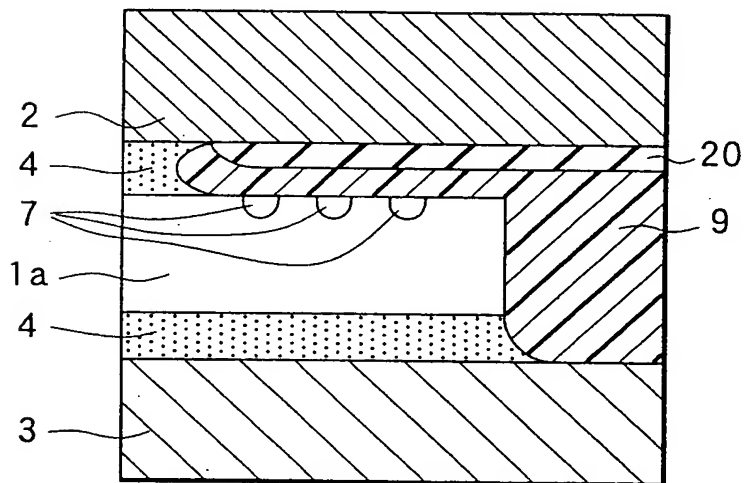
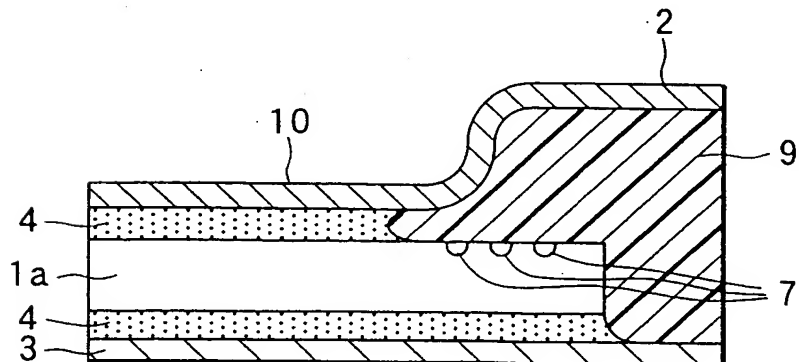


FIG. 9C





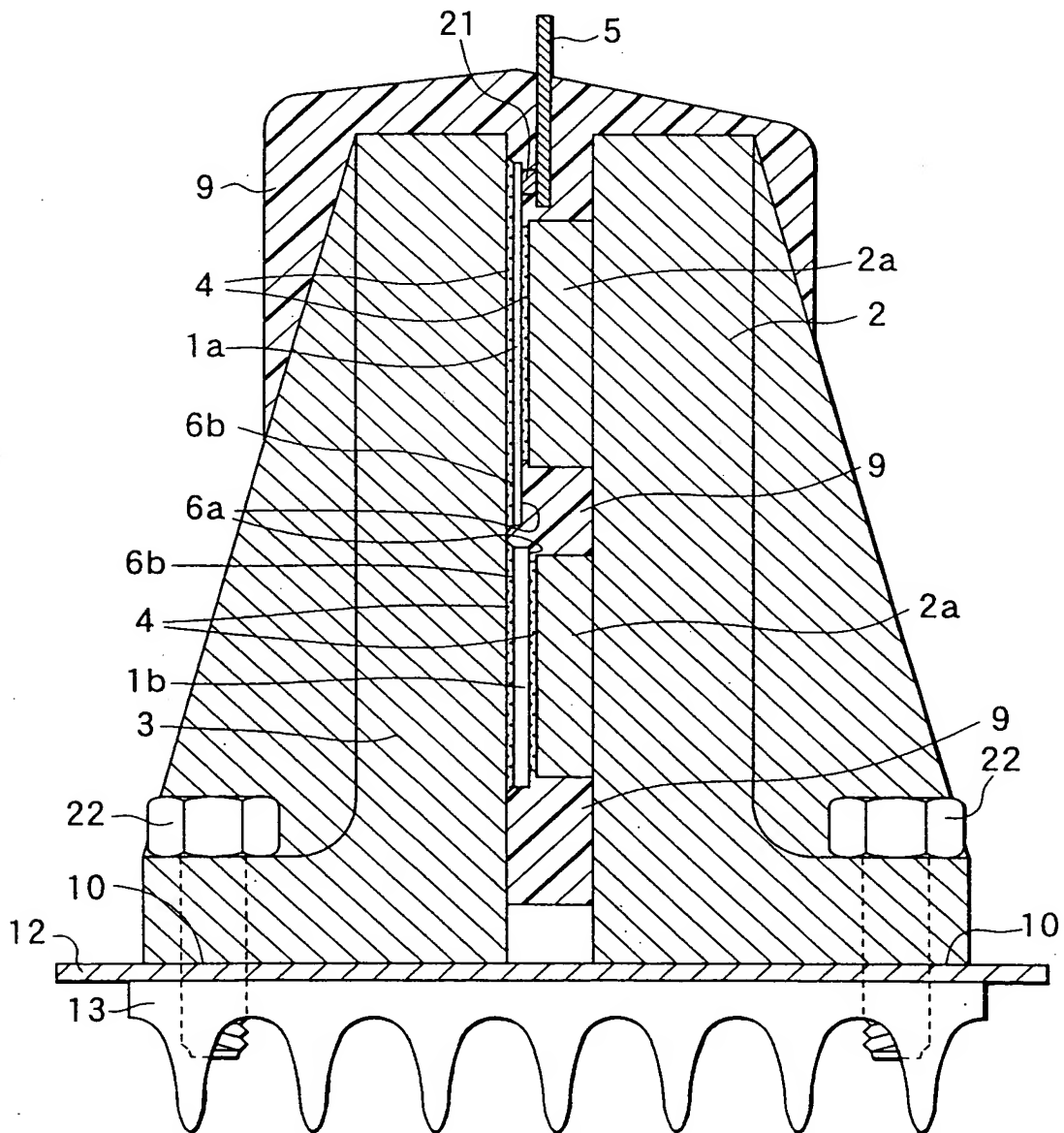
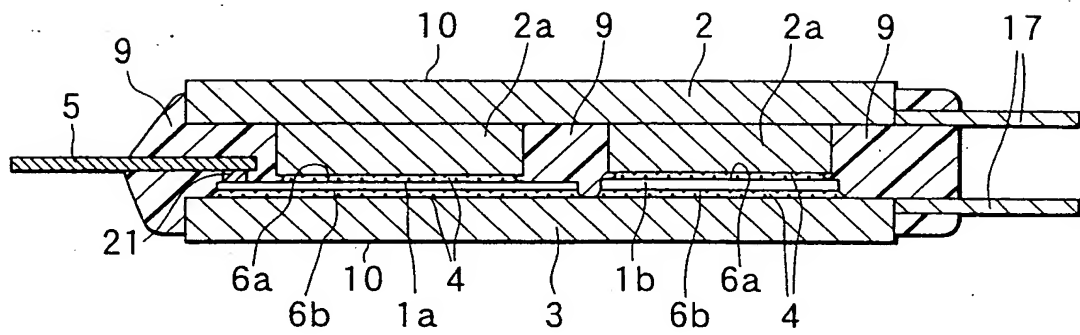


FIG. 12

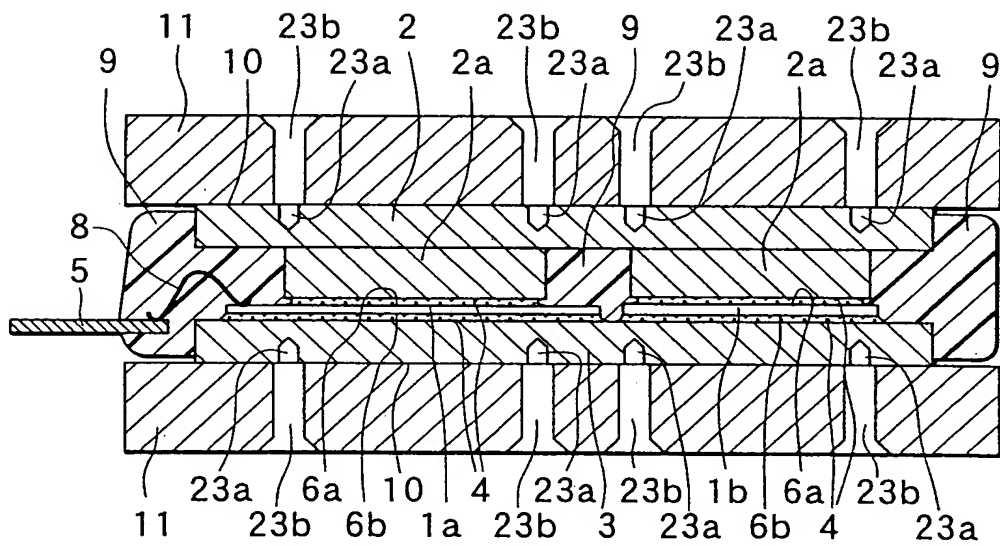
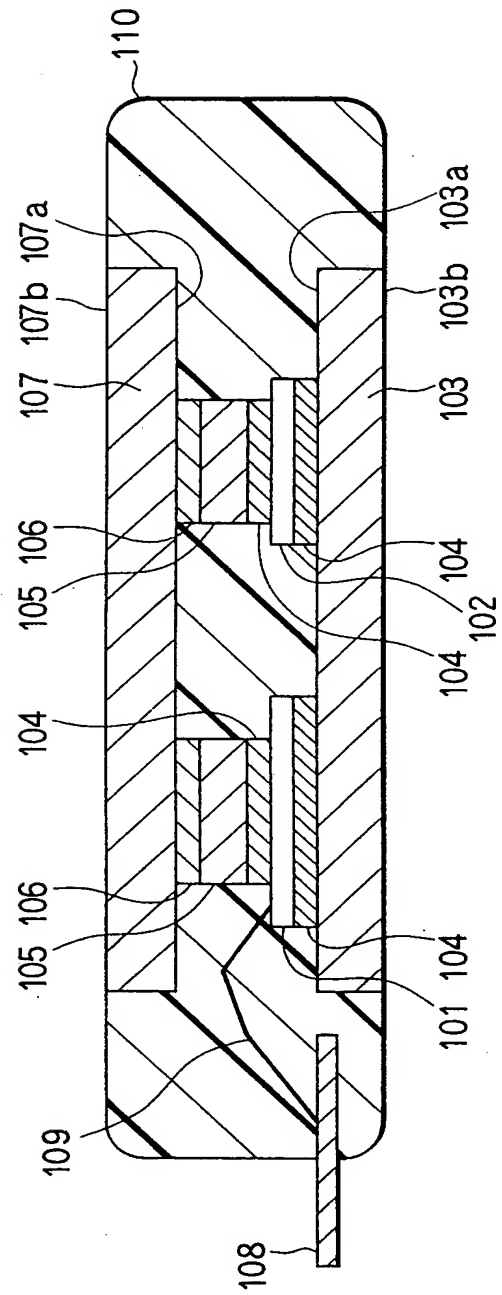
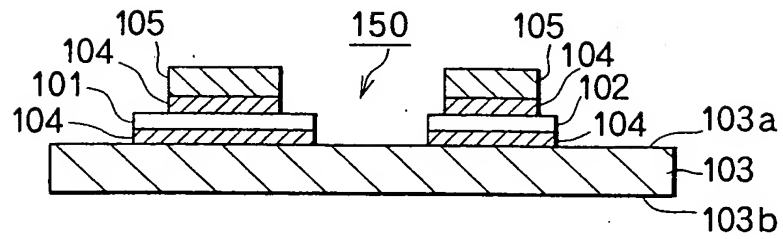


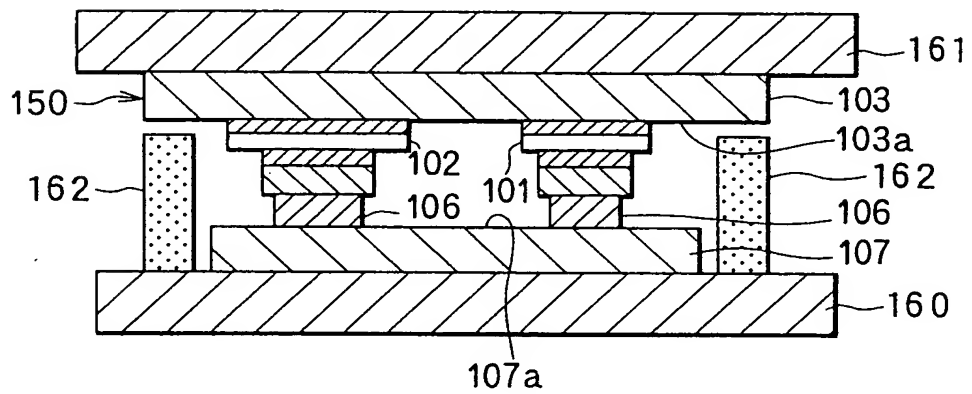
FIG. 13



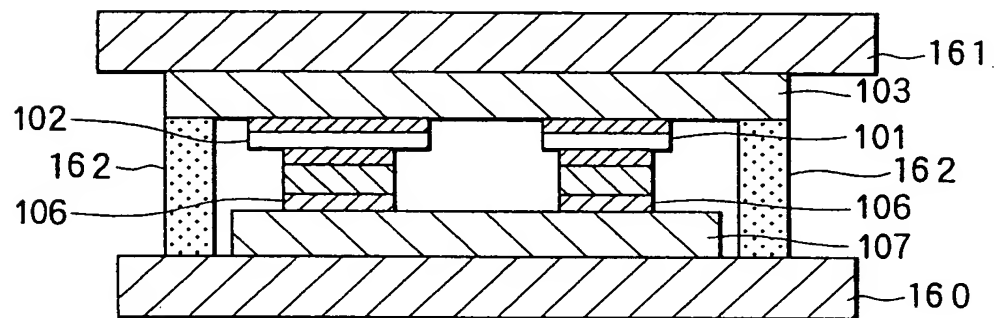
# FIG. 14A



# FIG. 14B



# FIG. 14C



# FIG. 15

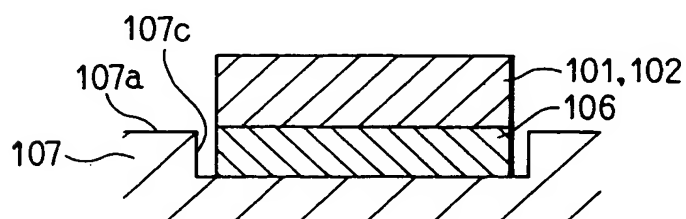
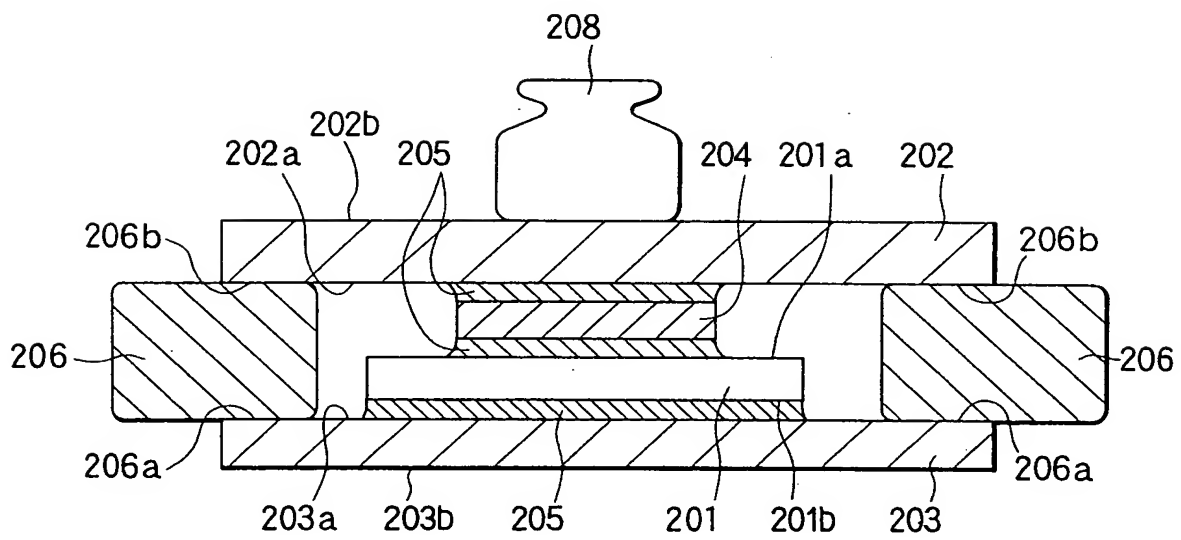
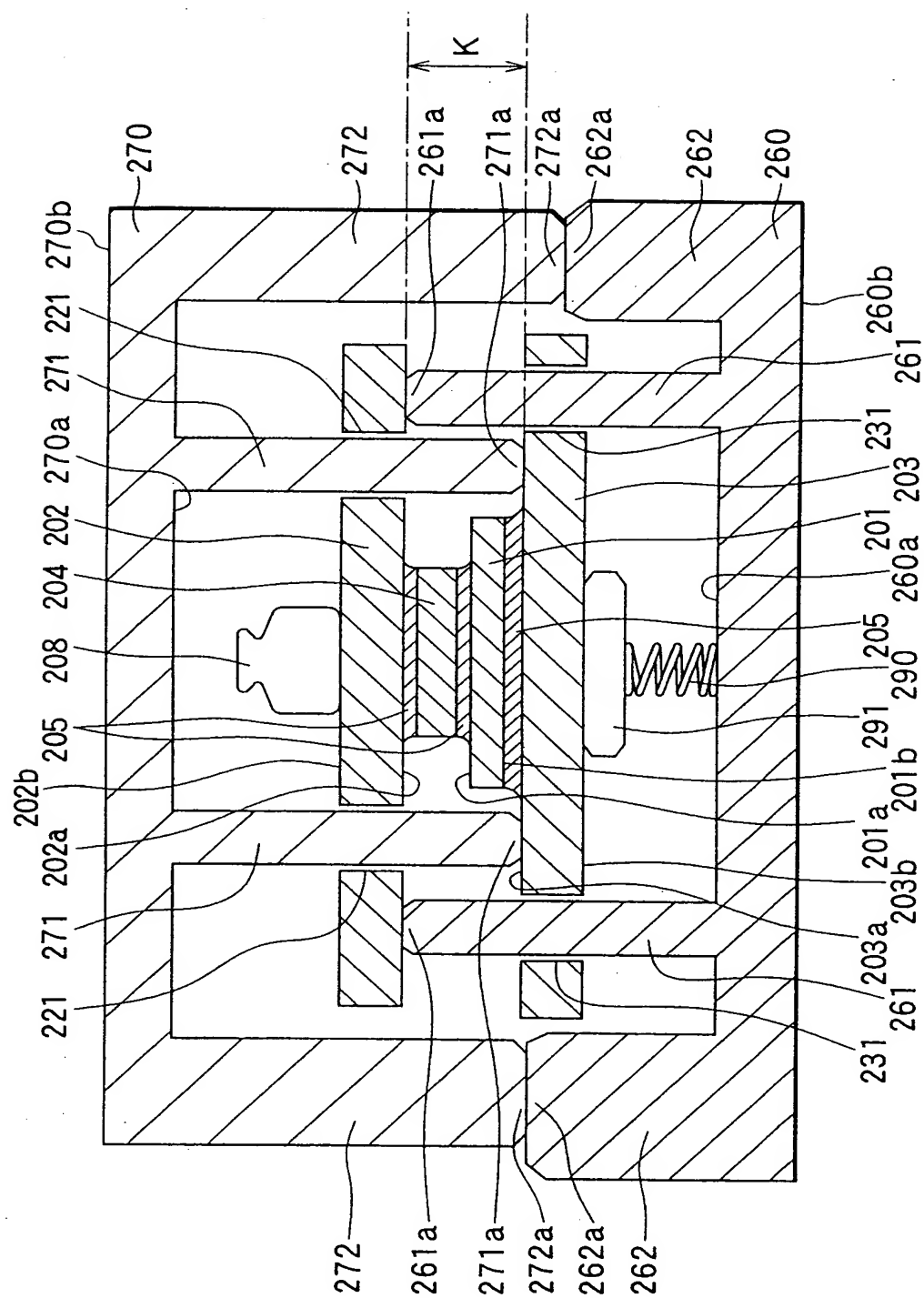


FIG. 16





816 F.

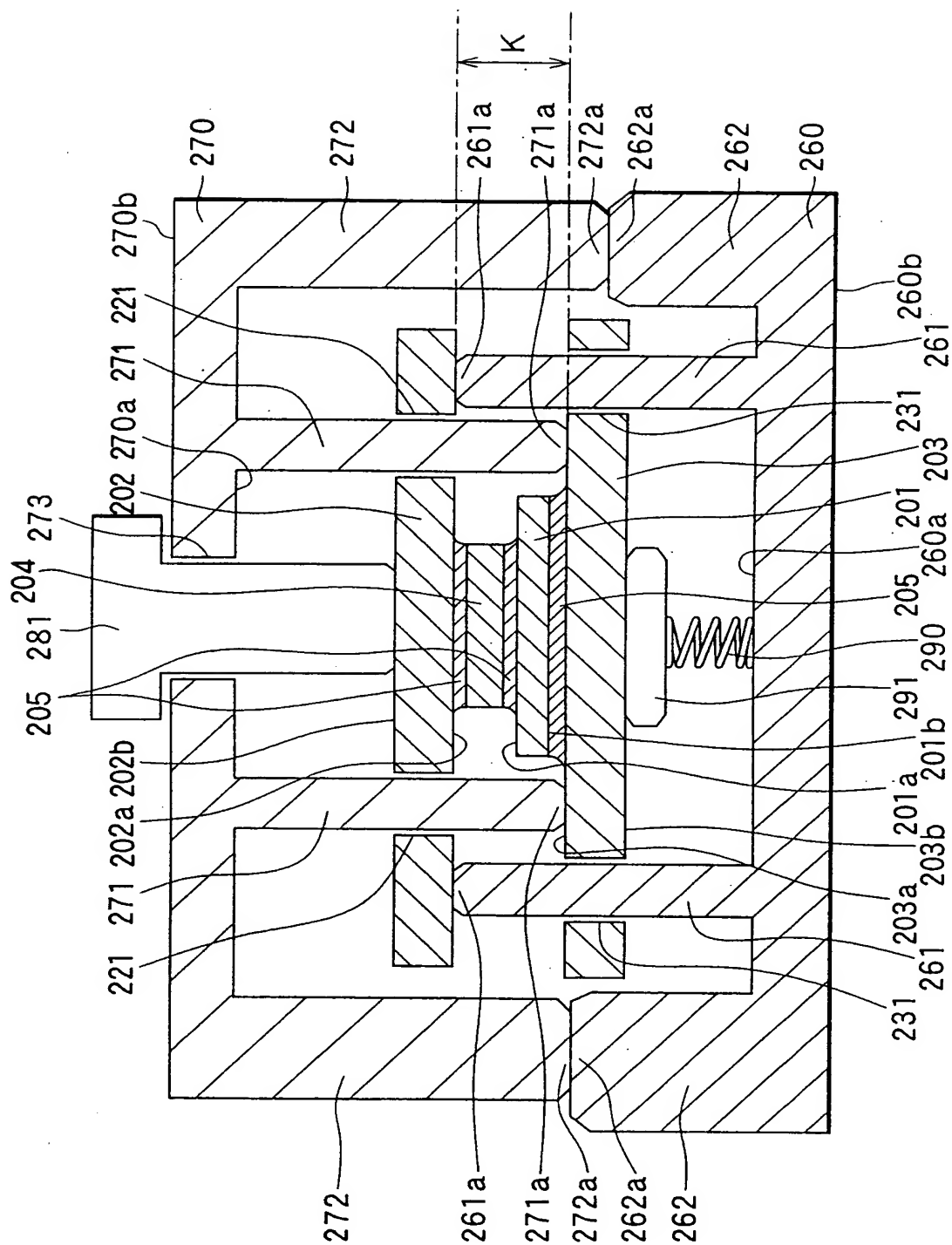
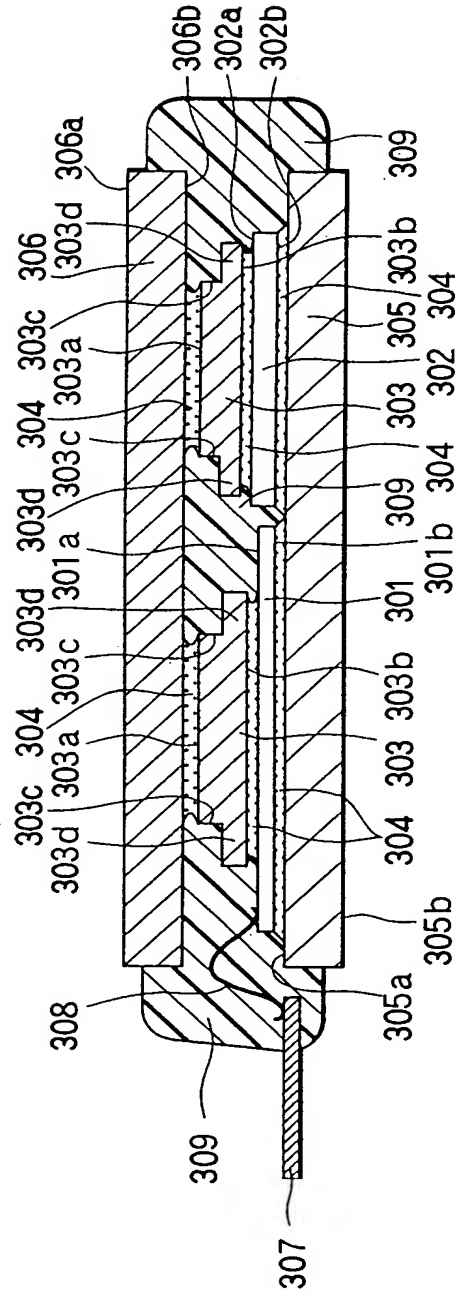
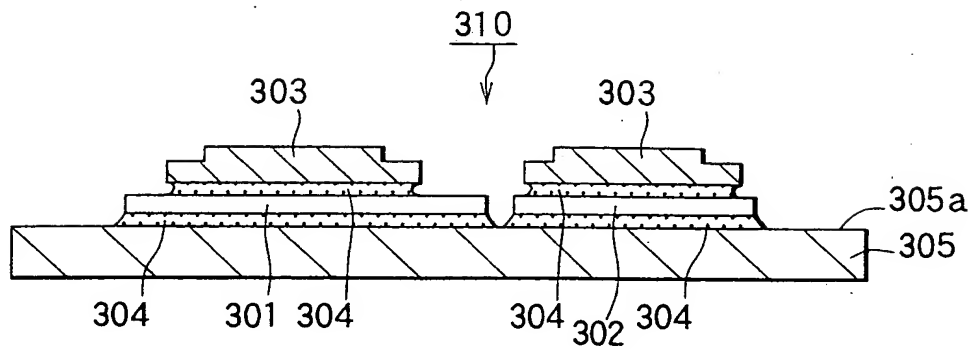


FIG. 19

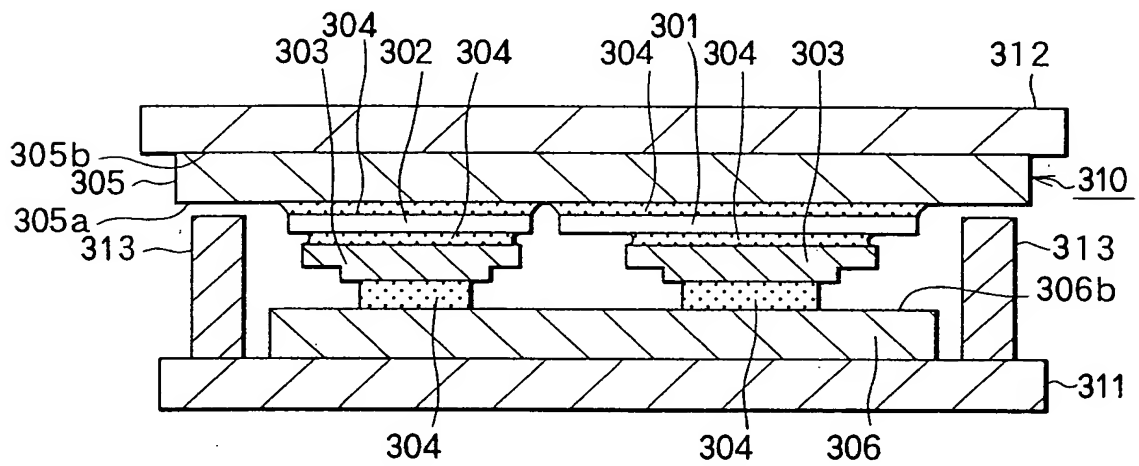




# FIG. 20A



# FIG. 20B



# FIG. 20C

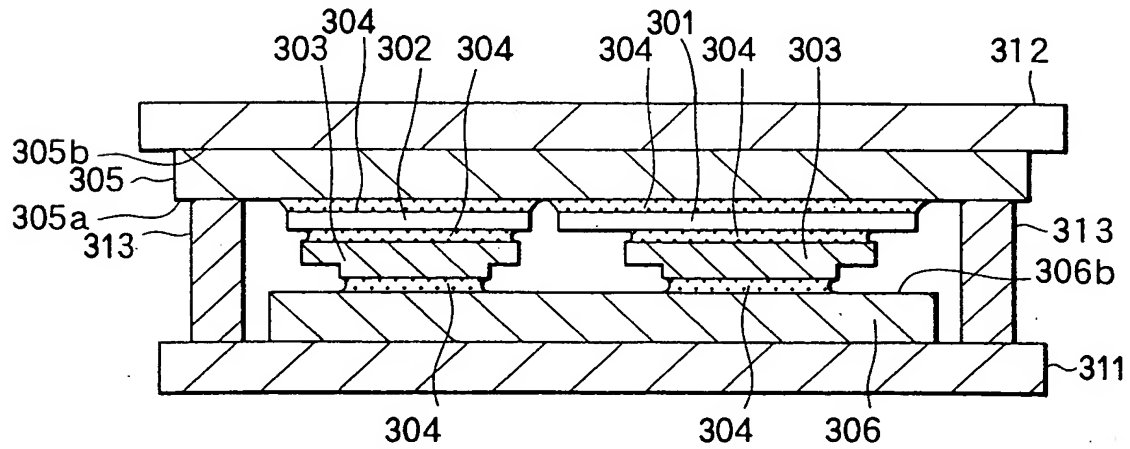


FIG. 21

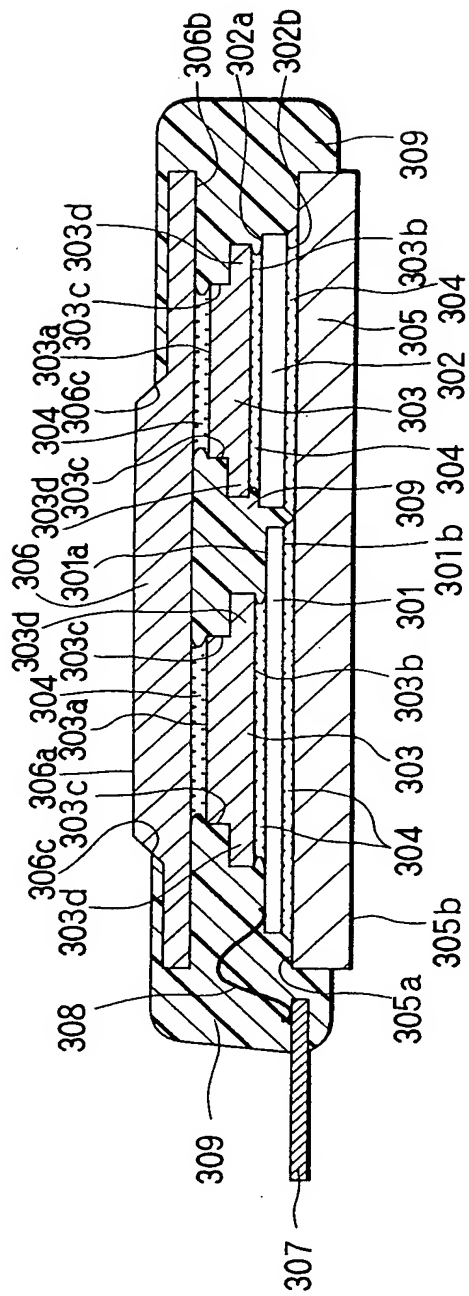
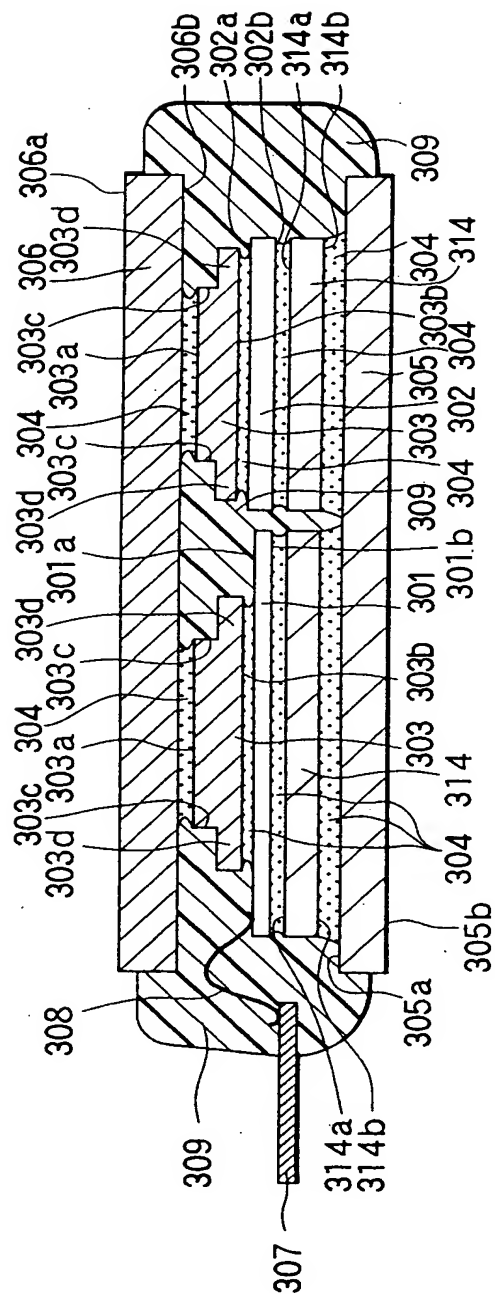


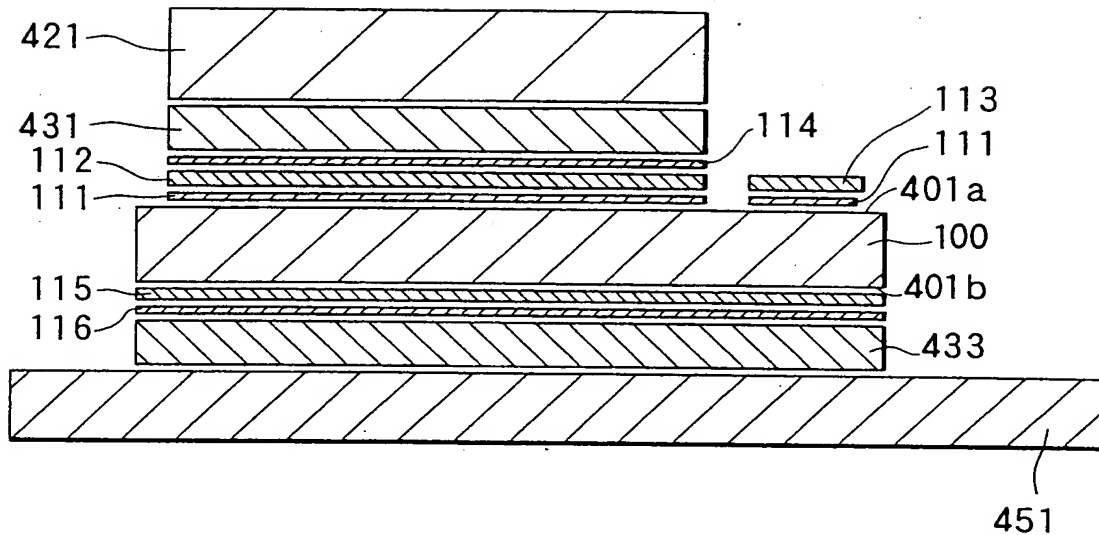
FIG. 22



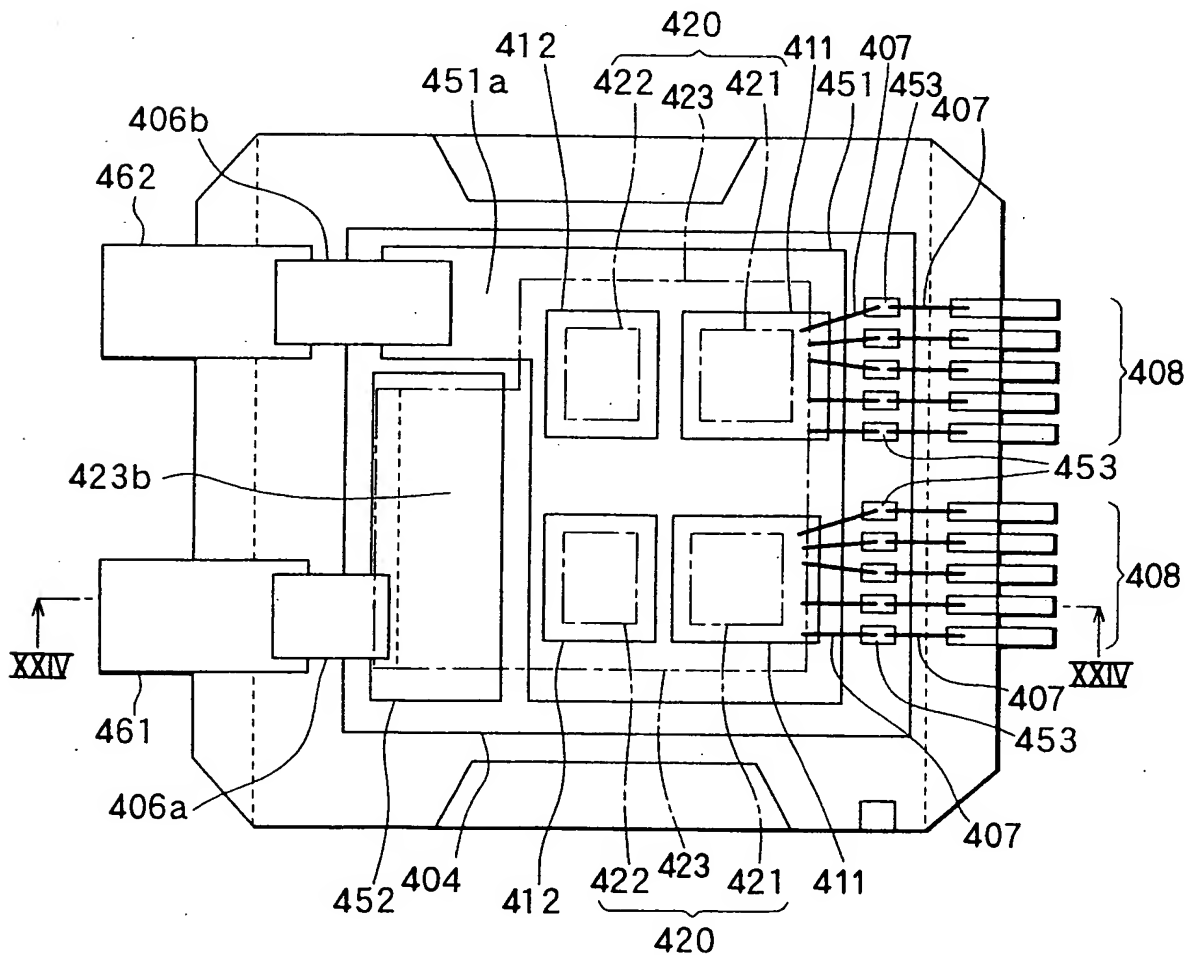
XXVI

461 423b 423 420 422 432 431 XXV 411 408 404 400 407 421 432 401a 431 412 434 423a 406a 405a 405b 405 452 424 433 451 401b 433 435 409 453 454 455

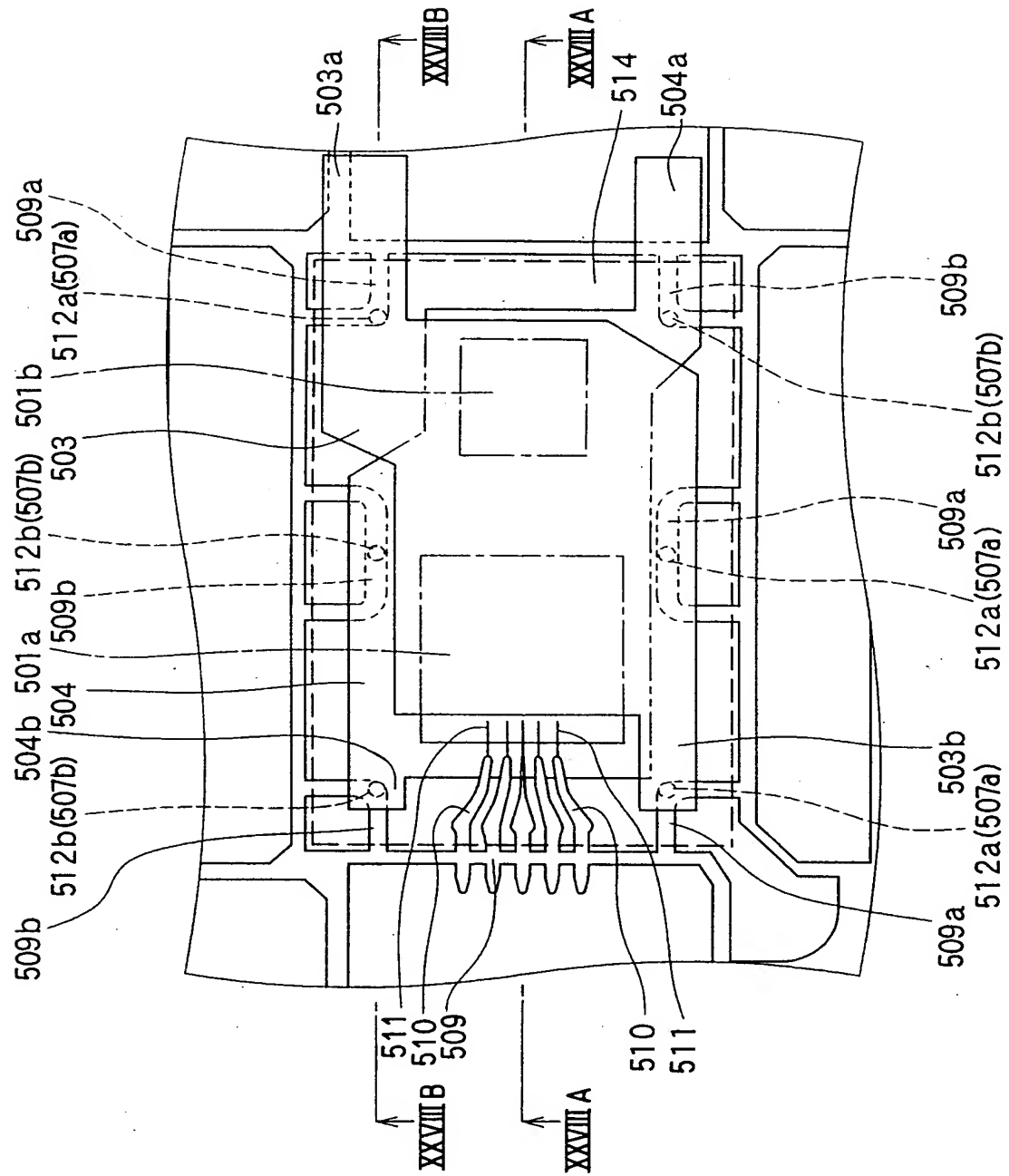
# FIG. 25



# FIG. 26



# FIG. 27



[illegible]

FIG. 30A

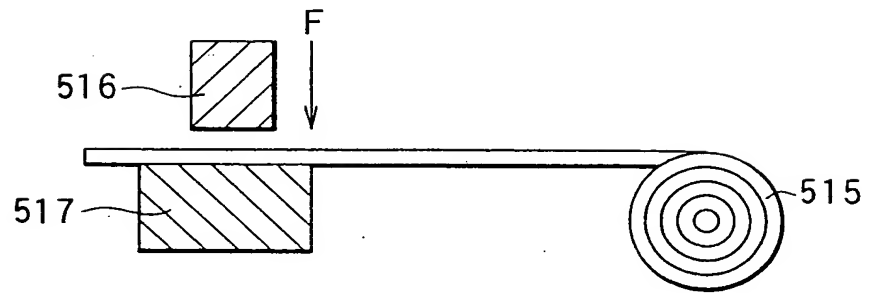


FIG. 30B

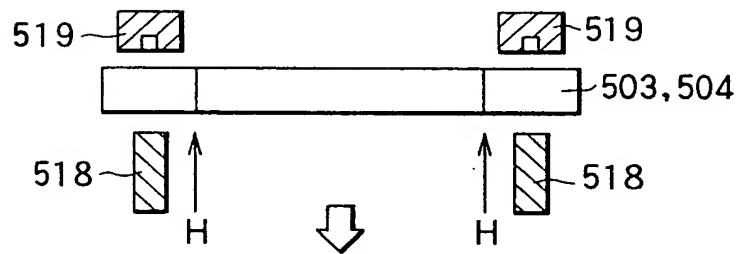


FIG. 30C

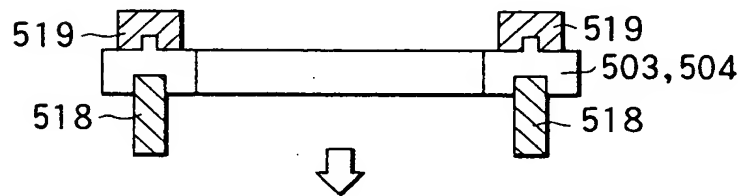
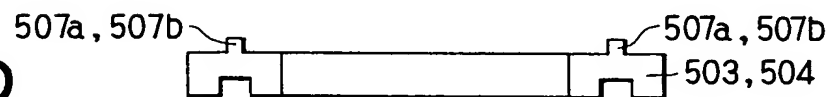


FIG. 30D

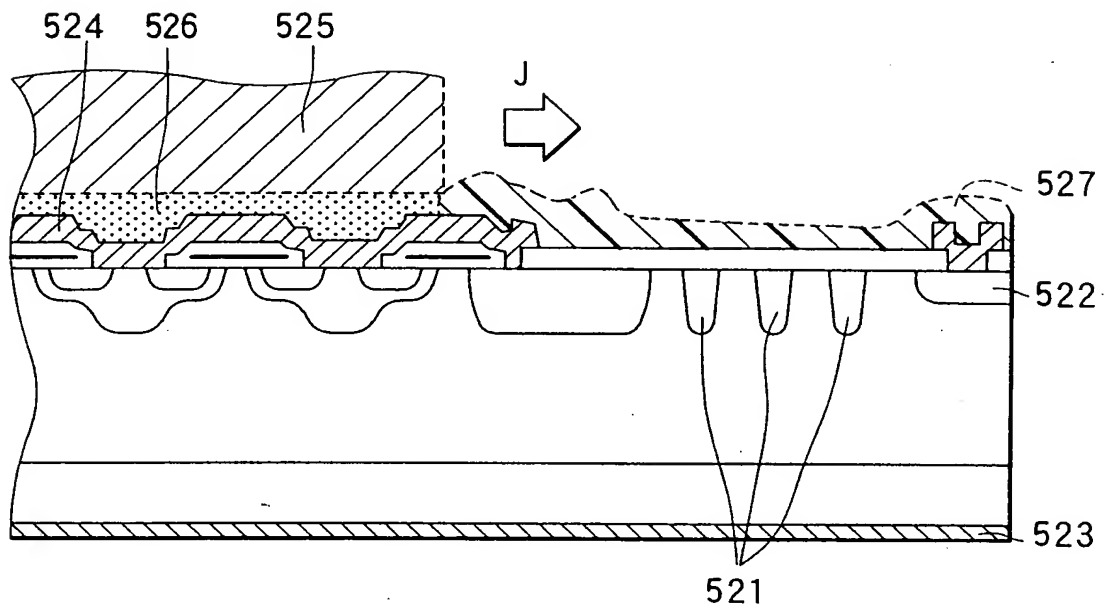


[illegible]

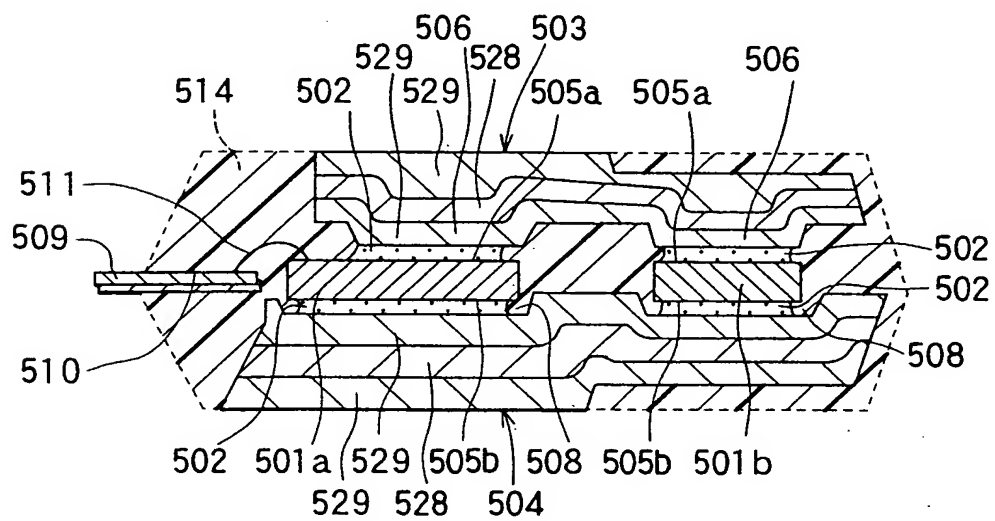
This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 503 with a top surface 504. A layer 509 is formed on the top surface 504. Two gate electrodes, 512a and 512b, are formed on the top surface 504. Two source/drain regions, 507a and 507b, are formed in the layer 509. The gate electrodes 512a and 512b are positioned over the source/drain regions 507a and 507b, respectively.



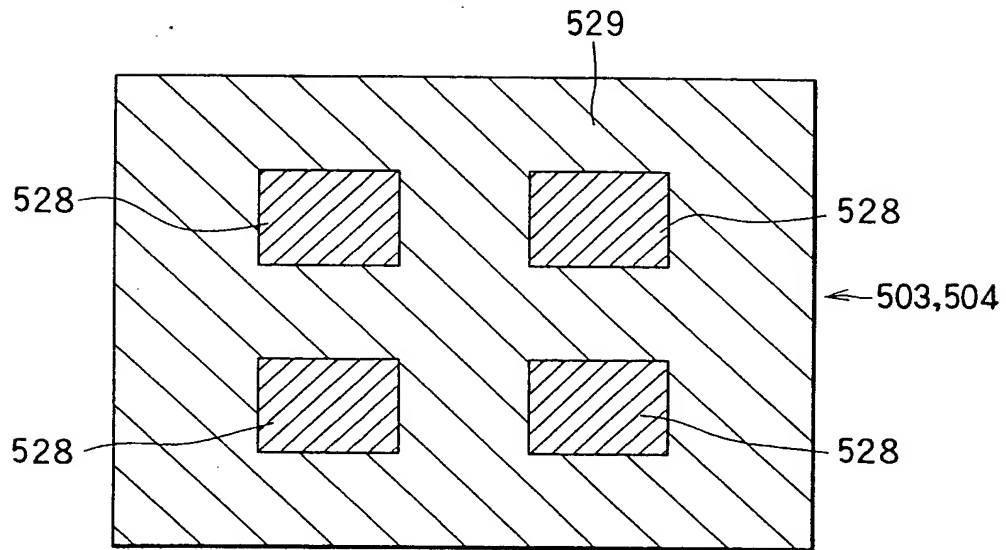
# FIG. 33



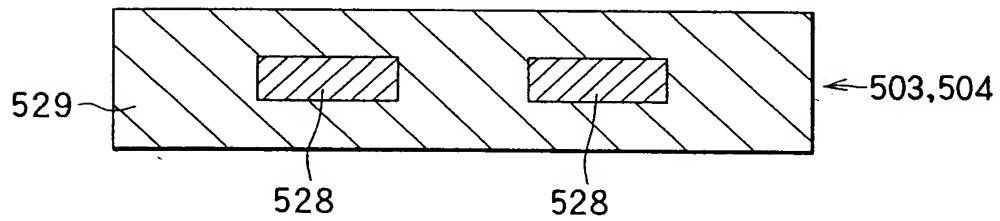
# FIG. 34



# FIG. 35A



# FIG. 35B



# FIG. 36

